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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,195	05/20/2004	Karl M. Guttag	KAGU-0002-UTY	7299

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EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/849,195	GUTTAG ET AL.	
	Examiner	Art Unit	
	Prabodh M Dharia	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-168* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-168* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged.

Applicant's specific reference to the earlier filed application is acknowledged.

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because it repeats the title. Correction is required. See MPEP § 608.01(b).

Election/Restrictions

4. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-14 are drawn to display driving by controlling light modulating element, classified in class 345, subclass 85-87.

II. Claims 16-29,142,143 are drawn to display, with series of stages each having stage value corresponding to pixel value of light modulating element, classified in class 369, subclass 44.12.

III Claims 30-38 are drawn to display with storage bits corresponding to pixel value of light modulating element and mask write operation as updating means which also performs setting and resetting in class 345 subclass 100.

IV Claims 39-47 are drawn to display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element, classified in class 385 subclass 9 and 19.

V Claims 48-67 are drawn to display with logical bit serial operation such as arithmetic, classified in class 378 subclass 62.

VI Claims 68-89 are drawn to two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value, classified in class 436 sub class 43.

VII Claims 90-125 are drawn to method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator, classified in class 353 sub class 20 and class 345 sub class 467.

VIII Claims 126-130 are drawn to digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, classified in class 701 sub class 213-215.

IX Claims 131-141 are drawn to array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, classified in class 708 sub class 130.

X Claims 144-157 are drawn to a spatial light modulator comprising an array of master slave bit pair stored in MRAM, classified in class 714 sub class 31,800.

XI Claims 158-160 are drawn to Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference, classified in class 347 sub class 239,241.

XII Claims 161-168 are drawn to MRAM array storage bits arranged in MRAM columns, classified in class 711 sub class 163 and class 359 sub class 244.

5. The inventions are distinct, each from other because:

Invention I relates a display unit driving by controlling light modulating element; however, it does not relate to display with logical bit serial operation such as arithmetic, spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference or series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM.

Invention II relates relate series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator; however, it does not relate to display with logical bit serial operation such as arithmetic, reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair

stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention III relates to display with storage bits corresponding to pixel value of light modulating element and mask write operation as updating means which also performs setting however, it does not relate to stage value corresponding to pixel value or providing memory on a spatial light modulator; reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention IV relates to display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element, however, it does not relate to display unit driving by controlling light modulating element; stage value corresponding to pixel value or providing memory on a spatial light modulator; reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention V relates to display with logical bit serial operation such as arithmetic, however, it does not relate to display unit driving by controlling light modulating element; stage value corresponding to pixel value or providing memory on a spatial light modulator;

reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention VI relates to two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value, however, it does not relate to display with logical bit serial operation such as arithmetic, spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference or series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM.

Invention VII relates to method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator, however, it does not relate to digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements.

Invention VIII relates to digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, however, it does not relate to method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, a spatial light modulator comprising an array of master slave bit pair stored in MRAM, or two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value.

Invention IX relates to array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, however, it does not relate to Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference, a spatial light modulator comprising an array of master slave bit pair stored in MRAM, or MRAM array storage bits arranged in MRAM columns.

Invention X relates to a spatial light modulator comprising an array of master slave bit pair stored in MRAM, however, it does not relate to display with logical bit serial operation such as arithmetic, digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, method comprising of providing memory on a spatial light modulator; and reallocating available memory

for data on spatial light modulator or display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element.

Invention XI relates to Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference, however, it does not relate to display with logical bit serial operation such as arithmetic, digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator, display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element or MRAM array storage bits arranged in MRAM columns; series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator.

Invention XII relates to MRAM array storage bits arranged in MRAM columns, however, it does not relate to a display unit driving by controlling light modulating element; Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference, a spatial light modulator comprising an array of master slave bit pair stored in MRAM, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, method comprising of providing memory on a spatial light modulator; and reallocating available memory

for data on spatial light modulator; two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value.

6. These above mentioned reasons the inventions described and categorized by class /subclass above are distinct. Search required for each class and subclass is independent.

7. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

8. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement is traversed (37 CFR 1.143).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 703-605-1231. The examiner can normally be reached on M-F 8AM to 5PM.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-3054938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

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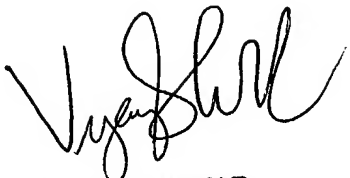

VIJAY SHANKAR
PRIMARY EXAMINER